REMARKS

Claims 1 through 20 remain pending in this application. In response to the Office Action dated March 26, 2003, the specification and claims 2, 3 and 19 have been amended. Care has been taken to avoid the introduction of new matter. Favorable reconsideration of the application in light of the following comments is respectfully solicited.

An Information Disclosure Statement, citing two references was filed April 17, 2001. A certified copy of priority papers in support of a claim for foreign priority was filed on the same date. Acknowledgement of these documents is respectfully requested.

Objection has been made to the drawings for the reason that reference numerals 38, 248, 54, 68, 74, 76 and 80 are not mentioned in the specification. In response, the specification has been amended at page 2 to reference the input/output buffer 248. With respect to the remaining identified reference numerals, it is submitted that each appears identified in the specification. For example, reference numeral 38 appears at page 1, line 33, reference numeral 54 at page 10, line 2, reference numeral 68 at page 18, line 3, reference numeral 74 at page 18, line 12, reference numeral 76 at page 18, line 23, and reference numeral 80 at page 17, line 30. As like elements have like reference numerals throughout the drawings, it is submitted that the objection should be withdrawn.

Claims 2 through 10 have been rejected under the second paragraph of 35 U.S.C. § 112. In response, the phrases "said instruction memory," in claim 2 at lines 5-6 and in claim 3 at line 2, have been amended to recite " said rewritable instruction memory" as required in the Office Action. The rejection, thus, has now been overcome; withdrawal of the rejection is respectfully solicited.

Claims 1 through 20 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. patent 5,974,579 (Lepejian) as set forth at length at pages 3-7 of the Office Action.

Independent claim 1 expressly recites "a select circuit selectively applying to said memory cell array test data applied from said test circuit and data applied from said input buffer according to whether in a test operation or a normal operation." It is submitted that the statement of the rejection does not identify a specific portion of Lepejian that discloses this claimed requirement nor can such feature be found or suggested in the reference.

The select circuit defined in claim 1 switches between a signal applied from the ATE external to the memory device and a signal from the BIST circuit with a programmable ALPG in the device. The signal (from ATE or BIST circuit) applied to the select circuit is a command control signal to control the memory device or an address signal addressing a memory array, not the data written/read out with respect to the memory array. By virtue of this select circuit, the cost required for testing facilities such as ATE can be suppressed even if the storage capacity of the memory device is increased in a test mode by conducting a test using the internal BIST circuit. Also, since the BIST circuit connected by the select circuit is a programmable BIST circuit, a desired test pattern can be generated as the ATE even after the fabrication process (after the wafer process).

Lepejian teaches that a multiplexer is provided at the memory input/output line so that the data read out from the memory can be returned, when the memory is in a test mode, to an adjacent bit in a subsequent writing operation. Multiplexer 45 in Lepejian device functions to switch so as to increment or decrement the sequence of the address generated by an address generation circuit 40, and is completely different from the select circuit of claim 1 in the present invention. As there is no teaching that would have motivated an artisan to modify Lepejian, withdrawal of the rejection of claim 1 and its dependent claims 2 through 16 is respectfully solicited.

Independent claim 17 is directed to a method of loading to an instruction memory that stores the instruction to the ALPG generating a memory test pattern. Loading is terminated when there is a data end instruction in the loading data. The feature is provided to quickly end the loading when the data to be loaded (memory test pattern generated by ALPG) is short to reduce the overhead time required for test preparation. In a BIST with a programmable ALPG as in the present invention, the method of reducing the time required to load into an instruction memory is an important distinction. Lepejian does not disclose such an instruction memory. Withdrawal of the rejection of claim 17 and its dependent claim 18, therefore, is respectfully solicited.

Independent claim 19 requires read out from a memory cell array in synchronization with a first clock signal of a first frequency to an external circuit that operates in synchronization with a second clock signal of a lower frequency. Dependent claim 20 is directed to scrambling the address so as to exchange the order of data output from the device, facilitating determination at the ATE side of low speed in the case where the output of a memory device operating at high speed in independent claim 19 is determined using the low speed ATE. If this feature is not present at the device (BIST) side, determination at the ATE side is rendered difficult. This means that AT speed testing which is a test that operates the memory device at a higher speed than the ATE cannot be realized. Although the ATE for a memory generally has an address scramble function, the scramble cannot be altered by the writing or reading operation with respect to the device. This feature is employed since information of errors corresponding to the address in the memory device must be taken in the ATE in order to conduct remedy analysis of the memory device having redundancy. As Lepejian lacks teaching or suggestion of these features, withdrawal of the rejection of claims 19 and 20 is respectfully solicited.

In summary it is submitted that the application as amended overcomes all objections and rejections of record. Allowance of the application is respectfully solicited.